A High Speed Low Input Current Low Voltage CMOS Current Comparator

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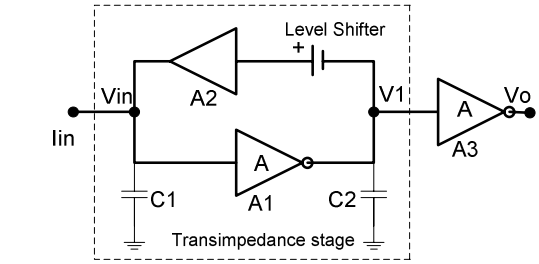
ABSTRACT

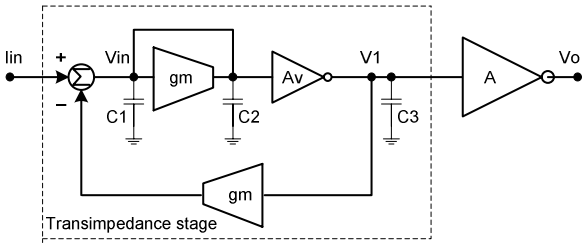
A new high speed low input current comparator is proposed in this paper. Based on a simple negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain, the transformed voltage signal is maintained at the lowest swing that results in a speed improvement. On a 0.25um TSMC CMOS process, simulation results demonstrate propagation delays of 3.6ns with ±100nA input current and 1.5Volts power supply, while the smallest input current is ±50pA. Performances are also shown with other V_{DD} such as 1.0, 1.8 Volts.

1. INTRODUCTION

In the last decade, current-mode circuits [1]-[3] have drawn lots of interest for modern integrated circuits and sensory systems. This is due to their attractive features such as high speed, wide dynamic ranges and low voltage operation, all of which are mainly due to the fact that all node voltages swing are very low. In analogue and mixed signal processing, the current comparator is also one of the key elements. The circuit is not purely in a current-mode operation since although the input signal is current the output signal is digital logics or rail to rail voltage signal. Obviously there is a requirement to transform the input current to a large voltage signal. Thus to design a high speed current comparator, one has to take care of the voltage swing carefully since it directly determines the propagation delay. Conventionally, most reported current comparators [4]-[7] are based on the concept shown as a block diagram in Figure 1(a), where the input current signal is converted to the voltage V_{in} and V_1 by the transimpedance stage comprising inverter amplifier A_1 and voltage buffer A_2. The resulting voltage V_1 is then amplified by the latter high gain inverter amplifiers A_3 to produce output logic voltage. There exist parasitic capacitors at all nodes. Ideally for high speed comparators, the signal swing at V_1 should be maintained as small as possible and situated exactly around the inverter threshold voltage of the inverter A_3. However, the reported works were relating to improve the lowest input current acquiring ability by arranging a proper biasing to turn on the MOSFETs of the buffer A_2 all the time. Most of them utilized diode connected MOSFETs as a level shifter to create V_{GS} of the buffer MOSFETs. It is seen that although the transimpedance stage is formed in a negative feedback loop a much larger loop gain has not been exploited to keep the signal V_{in} and V_1 as low as possible. Moreover with a larger loop gain, the input impedance at node V_{in} could be much lower and receive a much smaller input current in the pico Amps range. The so called dead zone which is the smallest input current range to which comparators are insensitive is then minimized. However, a drawback of having the small voltage swing at V_1 is that the gain of the latter inverter amplifier must be necessarily high with hence a higher power consumption. Obviously, there is a conflict that if a speed as a result of a small voltage swing of the tranresistance stage is desired, a very high gain of the latter inverter amplifier will be necessary to provide the rail to rail output swing. In this paper, we propose an idea based on Figure 1(b), where a much higher loop gain is emphasized to gain speed and then trade power to the latter high gain inverter amplifier. The circuit utilizes only CMOS inverters and is suitable for a low V_{DD} operation.



(a) Conventional



(b) Proposed

Figure 1 Current comparator concepts

2. THE PROPOSED CIRCUIT

As discussed above, we concentrate on a high speed or smallest average propagation delays and low input current acquiring capability or smallest dead zone. In this work, we trade off power for the required speed by maintaining the lowest voltage swing of the transimpedance stage and then providing high power to build up the latter high gain stage using inverter amplifiers. We then focus on the two separated circuit blocks as follows.

2.1 TRANSIMPEDANCE STAGE

The transimpedance stage, shown as the dashed block in Figure 2, plays the most important role in determining the speed of the comparator. It is seen that the whole stage is formed in a negative feedback loop by observing the polarities of output voltages and currents of each inverter. A_1 as a shorted input-output transconductance amplifier or inverter is basically an equivalent grounded resistor with the value of 1/gm. A_2 and A_3 are two high voltage gain amplifiers constructed from two cascaded inverters. Since there are two high impedance nodes in the loop RC frequency compensation is necessary to make the circuit stable. Capacitor C is set to 0.1pF while the resistor R is set to 1.6k Ohms. Note that the C and R could be made from a parasitic capacitor and a triode MOSFET respectively. The transconductance amplifier A_4 is used to provide negative feedback current to the input node. All amplifiers A_1 to A_4 are CMOS inverters designed with the same dimensions which are 2.1um/0.25um and 7um/0.25um for W/L of NMOS and PMOS respectively.

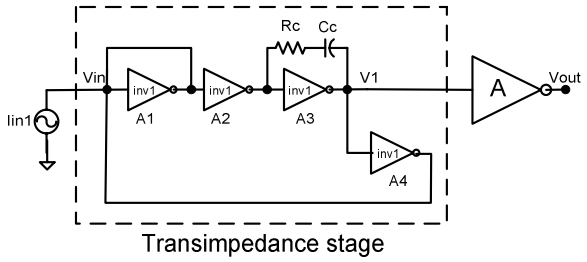


Figure 2 Transimpedance stage

Constructed in the feedback loop, the input resistance at node V_{in} can be derived as.

$$R_{in} = \frac{1}{gm_T}\frac{1}{\left(1+A_{vo}^2\right)} \qquad (1)$$

where gm_T is an equivalent transconductance of A_1 and and A_{vo} is a voltage gain of the amplifier A_2 and A_3. Note that all inverters have the same transconductance and voltage gain because they have the same dimensions. It is seen that the input resistance R_{in} is very small which results in a minimum voltage swing at node V_{in} and also the same value of V_1 at the output of A_3. Figure 3 shows an open loop gain and phase of the feedback current to the input current. It is seen that dc gain of 56dB, GBW of 906MHz and PM of 45° are achieved in the open loop transconductance stage. With this specification, we have enough loop gain to suppress signals for the lowest voltage swings at V_{in} and V_1 as shown in Figure 4. The negative feedback also stabilizes the common-mode voltage at all nodes to $V_{DD}/2$ which is set by the node V_{in}. This property is crucial for assuring that the signal swing is very small and also situated right at the center of the gate threshold voltage of the latter inverter of the gain stage.

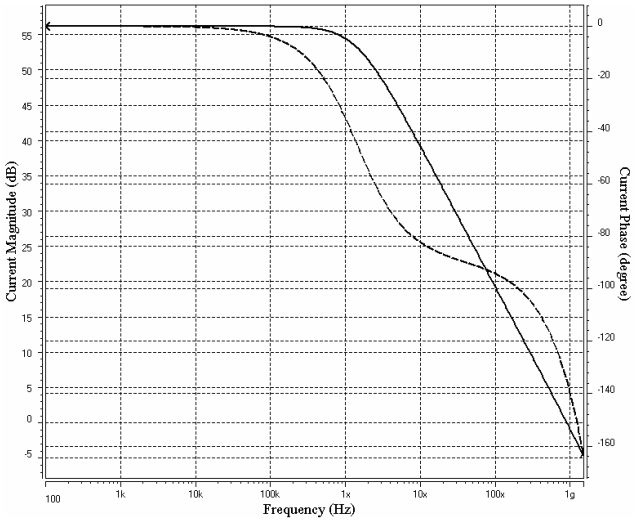


Figure 3 Open-loop responses of the transconductance stage

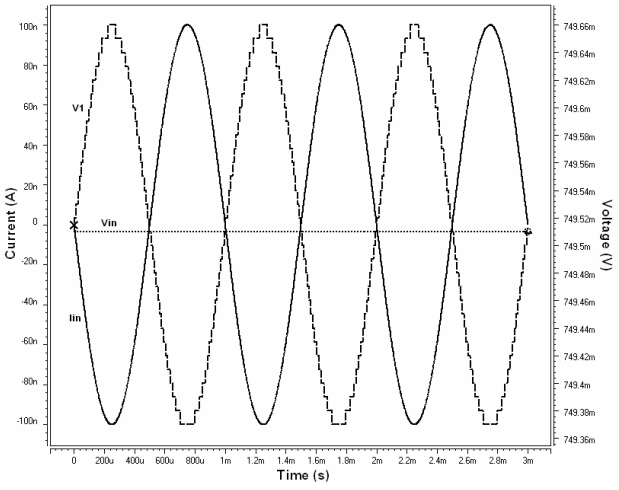


Figure 4 Voltage swings at V_{in} and V_1 vs. input current

2.2 GAIN STAGES

We have now a very small voltage swing V_1 at the input of A_5 of the gain stage. The main aim in designing this part is to construct high voltage gain to produce rail to rail output logic. Based on the use of the same dimension inverters, we can construct the high gain stage in a modular fashion.

INV1 has the same dimension as those in the transconductance stage. INV2 has smaller dimensions than those of INV1 by half, i.e. 1um/0.25um and 3.5um/0.25um for W/L of NMOS and PMOS respectively. The modules could be placed in parallel for higher gain. For A_5, there are six INV1s connected in parallel, where each INV1 possesses an output current equal to I_{in}. A_9 and A_{10} are only needed when I_{in} is lower than 10nA. Cascading many stages of the inverter does not deteriorate the speed much because each inverter has a very small propagation delay which is less than 1ns. So as discussed earlier the major contributor to the delay is the transimpedance stage.

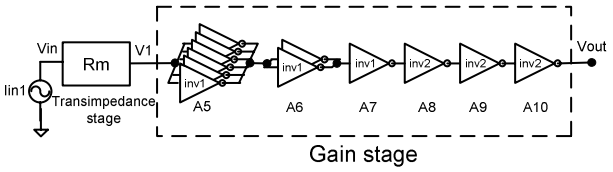
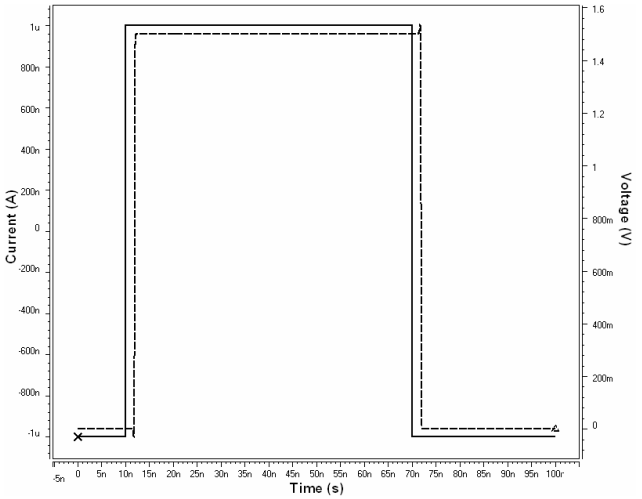


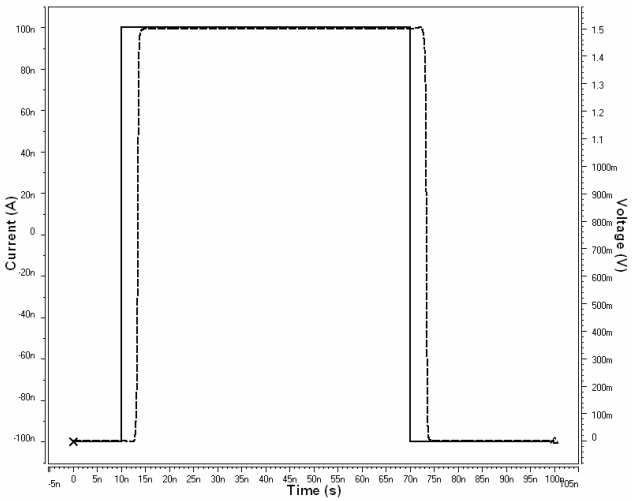
Figure 3 Gain stage

3. SIMULATION RESULTS

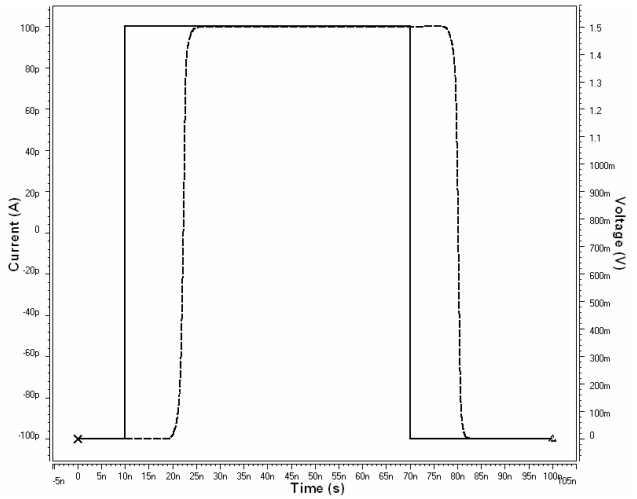
The proposed current comparator has been designed on a 0.25um TSMC CMOS process and tested with various power supplies and input current amplitudes. On HSPICE and with V_{DD} set to 1.5V, the comparator responses of three input current amplitudes of 1uA, 100nA and 100pA are shown in Figure 5 where the average propagation delays are 1.95ns, 3.6ns and 10.7ns respectively. Performances vs the input current amplitudes at 1.5V V_{DD} such as average propagation delay, static power and power delay product (PDP) are shown in Figure 6. It is seen that the lowest input current amplitude is at ±50pA thanks to the small input resistance as a result of the negative feedback with high loop gain. The average propagation delay is inversely proportional to the input current amplitudes since the voltage swing at the output of the transconductance stage is small. With small input current amplitudes, the static power also increases because all node voltages are around the common-mode value or $V_{DD}/2$ where most MOSFETs of the inverters are fully turned on. Propagation delays at various V_{DD} and input signal amplitudes are shown in Figure 7. Performance comparisons among many reported circuits are listed in Table 1. It is seen that the power is higher than those from some earlier designs because the scaling down of the V_{DD} normally degrades some properties of the inverter such as average drain current, voltage gain and propagation delay. Thus more power has to be pumped into the circuits in order to achieve the required speed and rail to rail output voltage swing.



(a) I_{in}=1uA

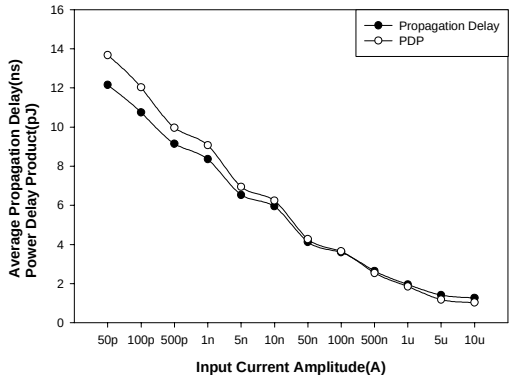


(b) I_{in}=100nA



(c) I_{in}=100pA

Figure 5 Transient Response of V_{OUT} vs. I_{in} at 1.5V V_{DD}



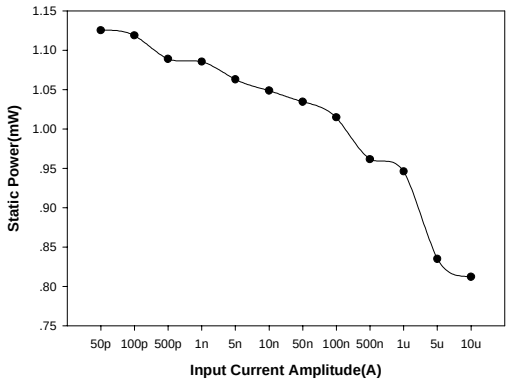


Figure 6 Performances at 1.5V V_{DD}

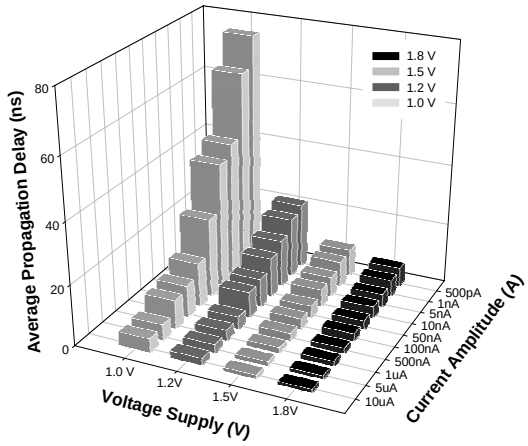


Figure 7 Propagation delays at V_{DD} 1.0-1.8 Volts

4. SUMMARY

A new high speed low input current low voltage current comparator has been demonstrated on a 0.25um TSMC CMOS process. Based on the concept of a high speed current-mode technique, we exploit a negative feedback scheme around the transimpedance stage with an emphasis on a very large loop-gain to produce a very small transformed voltage swing which is situated at the center of the gate threshold voltage of the latter stage. This will ensure the fastest response time. The same dimension inverters are used in all amplifier stages. They are fast and simple and suitable for low voltage operation. There is no extra biasing circuit and stacked transistor, thus the same design can be applied with various V_{DD} - ie there is no need to readjust the design.

5. REFERENCES

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Table 1 Performance comparisons

	Traff [4]	Tang [5]	Ravezzi[6]	Min [8]	Lin [7]	Proposed circuit		
Year	1992	1994	1997	1998	2000	2002	2002	2002
Power Supply (V)	5	5	5	3	3	1.5	1.0	1.8
Process (μm)	2	1.6	2.5	0.35	0.35	0.25	0.25	0.25
Minimum Input Current Amplitude (nA)	10	10	100	10	1	0.05	0.05	0.5
Propagation delay	±1μA/ 10ns	±0.1μA/ 11ns	±0.1μA/ 19ns	±0.1μA/ 7ns	±0.1μA/ 2.8ns	±0.1μA/ 3.5ns	±0.1μA/ 14.65ns	±0.1μA/ 2.6ns
Power consumption (mW) (at 0.1μA)	0.390	1.4	NA	0.45	0.58	1.01	0.022	2.73
PDP (pJ)	NA	NA	NA	3.15	1.4	3.648	0.32	7.25